* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the thin-film-semiconductor equipment which carried out accumulation formation of the bottom gate type TFT which makes polycrystal silicon etc. a barrier layer on the insulating substrate. It is related with the structure of the polycrystal silicon TFT created in a low-temperature process 600 degrees C or less in detail.
[0002]
[Description of the Prior Art] Thin-film-semiconductor equipment is suitable for drive substrates, such as an active matrix liquid crystal display, as an object for a display, and the development is furthered briskly now. Polycrystal silicon or amorphous silicon is used for the barrier layer of TFT. Especially polycrystal silicon TFT can realize small and high definition active matrix type electrochromatic display display, and attracts attention. In order to form TFT as a pixel switching element on the insulating substrate which consists of transparent glass etc., it is the technique of using for a barrier layer the polycrystal silicon thin film currently utilized only as an electrode material or an electrical resistance materials with the conventional semiconductor technique. It is the only technique in which the highly efficient TFT for switching elements in which the high-density design for realizing the picture image quality for which it is asked in a commercial scene is possible is realizable. This also enabled it to form simultaneously the circumference circuit section which used conventional external IC in the same process on the same substrate as the pixel array section. unrealizable in amorphous silicon TFT -- it is highly minute and the active matrix liquid crystal display of circumference circuit section one apparatus can be realized
[0003] Compared with amorphous silicon, since carrier mobility is large, the current drive capacity of polycrystal silicon TFT becomes high, and, as for polycrystal silicon, a high-speed drive can make simultaneously the circumference circuit sections, such as a required horizontal scanning circuit and a vertical-scanning circuit, on the same substrate as the TFT for pixel switching. Therefore, the number of books of the signal line taken out from the thin-film-semiconductor equipment for a display outside is sharply reducible. Moreover,-izing of the CMOS circuit which carried out accumulation formation of the N channel type and P channel type TFT can be carried out [on chip], built-in of a level shift circuit is attained and a low-battery drive of a timing system signal can be performed.
[0004] As the device technique and process technique of TFT, the elevated-temperature process technique which adopted the processing temperature of 1000 degrees C or more from the former is established. This elevated-temperature process feature is a point which reforms the semiconductor thin film formed on high thermal-resistance substrates, such as a quartz, by solid phase growth. A solid phase grown method is the technique of heat-treating a semiconductor thin film at the temperature of 1000 degrees C or more, and enlarges crystal grain of the piece piece contained in the polycrystal silicon which is a set of a minute silicon crystal in a membrane formation phase. As for the polycrystal silicon obtained by this solid phase grown method, the carrier mobility with high 100cm2 / v.s grade is obtained. In order to carry out such an elevated-temperature process, the adoption of a substrate excellent in thermal resistance is indispensable, and used the expensive quartz etc. from the former. However, the quartz is disadvantageous from the viewpoint of the formation of a manufacturing-cost reduction.
[0005] It replaces with the elevated-temperature process mentioned above, and the low-temperature process which adopted the processing temperature of 600 degrees C or less is developed. Laser annealing using the laser beam as part of the technique of forming the manufacturing process of thin-film-semiconductor equipment into a low-temperature process attracts attention. After this irradiates the semiconductor thin film of non-single crystals nature, such as amorphous silicon, polycrystal silicon, etc. which were formed on low thermal-resistance insulating substrates, such as glass, and carries out heating fusion of the laser beam locally at it, it crystallizes a semiconductor thin film by the cooling process. Accumulation formation of the polycrystal silicon TFT is carried out, using this crystallized semiconductor thin film as a barrier layer (channel field). Since the mobility of a carrier becomes high, the crystallized semiconductor thin film can carry out [highly efficient]-izing of the TFT to some extent.
[0006] By the way, top gate type structure of TFT is conventionally in use. On an insulating substrate, top gate structure forms a semiconductor thin film, and forms a gate electrode up through a gate insulator layer further. In a low-temperature process, the large-sized glass plate of a low cost is used for an insulating substrate. Since many impurity metals, such as Na, are contained in this glass plate, Na etc. localizes according to the voltage which drives TFT. There is a problem on the reliability of changing the property of TFT by the electric field. On the other hand, the bottom gate type structure where it was suitable for the low-temperature process in recent years is developed. On insulating substrates, such as a glass plate, this arranges the gate

electrode which consists of a metal membrane etc., and forms the semiconductor thin film through a gate insulator layer on it. It is effective in a gate electrode covering the electric field in a glass plate, and it compares with a top-on reliability gate type from a structural viewpoint, and the direction of a bottom gate type is excellent. Incidentally, the data which compared the reliability of the TFT of a bottom gate type and a top gate type are shown in drawing 7 . This data creates CMOS ring oscillator by TFT, and measures change of an oscillation frequency with time under a 120-degree C temperature condition. The direction of a bottom gate type compares with a top gate type, and the operating time current characteristic is stable so that clearly from the graph of drawing 7 .

[0007]

[Problem(s) to be Solved by the Invention] However, bottom gate structure has a big problem, when performing crystallization by laser annealing. The fraction from which the semiconductor thin film which carries out a recrystallization serves as a channel field in general is located in right above [of a gate electrode], and the fraction used as a source field and a drain field has it on a glass plate. When energy is given by irradiation of a laser beam for this reason, on a glass plate and a metal gate electrode, a difference comes out in the duction status and diffusion status of heat. Therefore, since the optimum laser energy differs in a channel field, a source field, and a drain field, the laser radiation in the optimum energy from which big carrier mobility is obtained becomes impossible. That is, on a metal gate electrode, although it is the translation which irradiates a laser beam simultaneously at both semiconductor thin film on a metal gate electrode, and semiconductor thin film on a glass plate when performing the recrystallization by laser annealing, while once melting-izing and solidifying by the cooling process, in order that heat may be transmitted and may diffuse a gate wiring horizontally, it solidifies comparatively for a short time. For this reason, on a metal gate electrode and a glass plate, the crystal grain of the semiconductor thin film which carried out the recrystallization differs, and carrier mobility becomes not uniform. If it says extremely, when it is going to enlarge the diameter of crystal grain of the semiconductor thin film on a metal gate electrode, irradiation energy becomes high too much and the semiconductor thin film on a glass plate may evaporate. Conversely, if it is going to normalize the crystallized state of the semiconductor thin film on a glass plate, as for the semiconductor thin film on a metal gate electrode, the diameter of crystal grain will become small. This has been the technical probrem which should solve the conventional bottom gate structure.

[0008]

[Means for Solving the Problem] The following meanses were provided in order to solve the technical probrem of a proior art mentioned above. According to this invention, thin-film-semiconductor equipment carries out accumulation formation of the TFT of the bottom gate structure which carried out the laminating of a gate electrode, an insulator layer, and the semiconductor thin film to order from the bottom on an insulating substrate as a fundamental configuration. As a characteristic feature matter, the aforementioned gate electrode has the multilayer structure which piled up the upper layer equipped with conductivity required in order that thermal conductivity may take a low contact comparatively at least, and the lower layer which thermal conductivity equipped with high and conductivity required as a wiring comparatively. The aforementioned semiconductor thin film has the polycrystal structure in which the recrystallization was carried out by energy irradiation in the status that it extended on this gate electrode and this insulating substrate through this insulator layer. Preferably, as for the aforementioned gate electrode, the cross-section configuration has the trapezoid. Moreover, at least the upper layer and one side of a lower layer of the aforementioned gate electrode are shading nature preferably.

[0009] According to other side faces of this invention, the thermally conductive substratum layer is formed so that the TFT of the bottom gate structure which carried out the laminating of a gate electrode, an insulator layer, and the semiconductor thin film to order from the bottom may be superficially seen in the front face of the aforementioned insulating substrate on an insulating substrate in the thin-film-semiconductor equipment which carried out accumulation formation and this gate electrode may be adjoined, and it is characterized by making uniform the heat-conduction status on the front face of an insulating substrate. In this case, the aforementioned semiconductor thin film has the polycrystal structure in which the recrystallization was carried out by energy irradiation in the status that it extended on this gate electrode and this substratum layer through this insulator layer.

[0010] According to the 1st side face of this invention, a gate electrode is made into a laminated structure and the upper layer equipped with conductivity required in order that thermal conductivity may take a low contact comparatively is formed. Thereby, the difference of the heat-conduction status is lessened on the insulating substrate the gate electrode top. Thereby, an optimization of laser energy is attained and a quality polycrystal semiconductor thin film can be obtained. Moreover, when thermal conductivity is low, it is common that electrical conductivity also becomes low according to this. This is a unfavorable conditions as a gate wiring. Then, by this invention, low resistance-ization is attained by preparing the lower layer equipped with conductivity required as a wiring. As mentioned above, what is necessary is just to make small the thermal conductivity of the conductor material used as a gate electrode, in order to cross all over an insulating substrate and to equalize a heat distribution. However, as a gate wiring, the method of resistivity of the parvus is as much as possible good. Since these two physical properties conflict, on the 1st side face of this invention, they make a gate electrode the two-layer structure, and use the upper layer and the good place of the physical properties of a lower layer. Moreover, according to the 2nd side face of this invention, the thermally conductive substratum layer is formed so that it may see superficially and a gate electrode may be adjoined, and the heat-conduction status on the front face of an insulating substrate is made uniform. Thereby, the recrystallization of the semiconductor thin film by laser annealing can be performed uniformly, and an optimization of laser beam irradiation conditions is attained.

[0011]

[Embodiments of the Invention] With reference to a drawing, the operation gestalt of this invention is explained in detail below. Drawing 1 is a typical fragmentary sectional view showing the 1st operation gestalt of the semiconductor thin film concerning this

invention. This thin-film-semiconductor equipment carries out accumulation formation of TFT 3 of the bottom gate structure which carried out the laminating of the gate electrode 5, the insulator layer 4, and the semiconductor thin film 2 to order from the bottom on the insulating substrate 1 which consists of glass etc. so that it may illustrate. This thin-film-semiconductor equipment is used for the drive substrate of active matrix type display. For this reason, the pixel electrode 14 is connected to TFT 3. Moreover, TFT 3 has double-gate structure, in order to raise a reliability. However, this invention cannot be overemphasized by that is not restricted to this and it can apply also to the TFT of single gate structure. In assembling display, it joins the insulating substrate 1 of another side to one insulating substrate 60 through a predetermined clearance. One insulating substrate 60 consists of glass etc., and the counterelectrode 61 is beforehand formed in the front face. Liquid crystal 50 is held as an electrooptic material in the clearance of both the substrates 60 and 1.

[0012] As a characteristic feature matter of this invention, the gate electrode 5 has the multilayer structure which piled up upper 5a and lower layer 5b at least. Upper 5a is equipped with conductivity required in order that thermal conductivity may take a low contact comparatively. Specifically, alloy layers, such as compound layers, such as ITO layer, TiN layer, and TiON layer, or Nichrome, are used. The thickness is about 50-300nm. On the other hand, lower layer 5b is equipped with the conductivity which thermal conductivity is high and needs it as a wiring comparatively. For example, low resistance high-melting point metal membranes, such as W, Cr, Mo, and Ti, are used. This thickness is in the domain of 50-200nm, for example, is set as 100nm. The gate electrode 5 is installed from the gate wiring (not shown). Generally, a gate wiring has the same multilayer structure as the gate electrode 5, and connects it to other circuit sections (not shown) through a contact hole (not shown). Upper 5a is equipped with conductivity required in order to take a contact at least by this relation, and lower layer 5b is equipped with conductivity required as a wiring. As for the gate electrode 5, the cross-section configuration has the trapezoid. The tilt angle of an end face is 45 or less degrees, and is in the domain of five - 15 degrees preferably. This trapezoid configuration is effective in order to prevent ****** of the layer formed more nearly up than the gate electrode 5. Moreover, either [at least] upper 5a or lower layer 5b is equipped with shading nature, and, as for the gate electrode 5, the gate electrode 5 is opaque collectively. This has suppressed the current leakage of TFT 3 by the light which carries out incidence from the rear face of an insulating substrate 1 etc.

[0013] the gate electrode 5 -- SiO2 etc. -- **** -- it is covered with the becoming insulator layer 4 On the insulator layer 4, the semiconductor thin film 2 which consists of polycrystal silicon etc. is formed. On the semiconductor thin film 2, patterning formation of the stopper 6 is carried out so that it may have consistency with each gate electrode 5. The fraction of the semiconductor thin film 2 located directly under a stopper 6 serves as a channel field. Moreover, the source field 7 and the drain field 8 where the impurity was poured in by high concentration are formed in the semiconductor thin film 2. Furthermore, the LDD fields 71, 78, and 81 where the impurity was poured in by low concentration are also formed. TFT 3 which has the starting configuration is covered with the layer mesenteriolum 9 which consists of SiO2 etc. On the layer mesenteriolum 9, patterning formation of the signal wiring 10 is carried out, and electrical connection is carried out to the source field 7 of TFT 3 through the contact hole. This signal wiring 10 has the two-layer structure of lower layer metal membrane 10b which consists of upper metal membrane 10a which consist of Mo etc., aluminum, etc. Similarly, patterning formation of the wiring 10 for connection is carried out at the drain field 8 side. These wirings 10 carry out a passivation membrane 11 in between, and are covered with the flattening layer 12. On the flattening layer 12, patterning formation of the pixel electrode 14 which consists of ITO etc. is carried out. Electrical connection of this pixel electrode 14 is carried out to the drain field 8 of TFT 3 through the wiring 10 for a contact hole and connection which carried out opening to the flattening layer 12.

[0014] With reference to drawing 2 , the manufacture technique of the thin-film-semiconductor equipment shown in drawing 1 is explained in detail. In order to see and translate ****, the gate electrode has shown only the piece. As first shown in (A), lower layer 5b is extensively formed by the spatter on the insulating substrate 1 which consists of glass etc. Since it is desirable that it is low resistance as for this lower layer 5b and it is desirable that it is a high-melting point further, generally metal membranes, such as W, Cr, Mo, and Ti, are used. A thickness is about 100nm. What is necessary is generally, just to go into the thickness domain of 50-200nm. Upper 5a is extensively formed by the spatter etc. continuously or nonsequetially on lower layer 5b. Besides, layer 5a serves as the characteristic feature element of this invention. Although there is no need that upper 5a is low resistance not much, the parvus material of heat conduction is used. However, it is necessary to have conductivity required even if upper 5a is unsuitable as a wiring, in order to take a contact. As for upper 5a, alloy layers, such as compound layers, such as for example, ITO layer, TiN layer, and TiON layer, or Nichrome, are used. The comparatively thicker one of a thickness is good and it is set as the domain which is almost 50-300nm.

[0015] Next, as shown in (B), patterning of the multilayer which piled up upper 5a and lower layer 5b is carried out by isotropic dry etching, and it is processed into the gate electrode 5. By performing isotropic dry etching, the cross-section configuration of the gate electrode 5 is processible into a trapezoid. Namely, as for the end face of the gate electrode 5, a taper is attached in five - 15 degrees.

[0016] As shown in (C), it is SiO2 with a plasma CVD method (PE-CVD). For example, it deposits by the thickness of 100-200nm, and considers as the insulator layer 4 which covers the gate electrode 5. Furthermore, on it, amorphous silicon is deposited by the thickness of 20-60nm, and the semiconductor thin film 2 is formed. Continuity growth of the insulator layer 4 and the semiconductor thin film 2 can be carried out, without breaking a vacuum by the same membrane formation chamber. Here, an insulating substrate 1 is heated to the temperature of 400 degrees C. About 10% of hydrogen is contained in the semiconductor thin film 2 of the amorphous silicon which formed membranes by PE-CVD, and it is desorbed from this hydrogen with heat treatment which is 400 degrees C. Then, XeCl excimer laser light with a wavelength of 308nm is irradiated, for

example, and the recrystallization of the semiconductor thin film 2 is attained. It becomes polycrystal silicon, when amorphous silicon carries out melting and becomes hard by the energy of a laser beam. Crystallinity (mainly the diameter of crystal grain, a grain size) is determined by this time when solidifying. In this invention, speed after using the material with comparatively small thermal conductivity, and the thermal diffusion of the Bunsui common orientation decreasing and carrying out melting as upper 5a of the gate electrode 5 until it solidifies becomes slow. The polycrystal silicon which sees practical by this and has a sufficiently big diameter of crystal grain is obtained. Moreover, since the gate electrode 5 is processed into the trapezoid configuration, it can prevent ****** of the semiconductor thin film 2 in the level difference section.

[0017] As shown in (D), it is SiO2 on the semiconductor thin film 2. It deposits by PE-CVD. Rear-face exposure technique is used here and it is SiO2. Patterning is carried out and it is processed into a stopper 6. That is, the stopper 6 adjusted in the gate electrode 5 by self-alignment can be obtained by performing rear-face exposure, using as a mask the gate electrode 5 which has shading nature. Here, an impurity (for example, Lynn) is comparatively poured into the semiconductor thin film 2 by low concentration by the ion doping method, using a stopper 6 as a mask. Furthermore, after covering a stopper 6 and its circumference with a photoresist, an impurity (for example, Lynn) is comparatively poured into the semiconductor thin film 2 by the ion doping method by high concentration. Thereby, the source field 7 and the drain field 8 are formed. Moreover, the LDD fields 71 and 81 of low impurity concentration are comparatively left behind the fraction of the semiconductor thin film 2 covered with the resist. Then, the photoresist which became unnecessary is removed. The ion doping method carries out the electric-field acceleration of the ion of the plasma state at a stretch, dopes it to the semiconductor thin film 2, and can be processed for a short time.

[0018] As finally shown in (E), in order to activate the doped atom, a laser beam is irradiated again. Although it is the same technique as a recrystallization, since it is not necessary to enlarge a crystal, weak energy is enough. Then, it is SiO2 because of the insulation during a wiring. It deposits and considers as the layer mesenteriolum 9. After carrying out opening of the contact hole to this layer mesenteriolum 9, metal aluminum etc. is deposited by the spatter, patterning is carried out to a predetermined configuration, and it is processed into wiring 10. Hereafter, in manufacturing the thin-film-semiconductor equipment for a display, it forms a passivation membrane, a flattening layer, and a pixel electrode if needed.

[0019] Drawing 3 expresses typically the temperature change of the semiconductor thin film at the time of laser annealing. In laser annealing, excimer laser light is irradiated in pulse, for example. The temperature of the silicon (Si) which constitutes a semiconductor thin film with pulse irradiation rises abruptly, and exceeds the melting point. After maintaining a steady state for a while after this, the temperature of Si falls gradually to a room temperature with an end of pulse irradiation. The once fused silicon solidifies at this time, and the polycrystal status is acquired. The cooling process is dependent on the thermal conductivity of the gate electrode of a substratum. As shown in a curve (1), when a gate electrode consists of the conventional single-level-metal layer, the temperature of silicon falls abruptly. On the other hand, as shown in a curve (3), the silicon on the insulating substrate which consists of glass etc. is cooled comparatively slowly. The thermal conductivity of this of glass is because it is low compared with a metal etc. The curve (2) expresses the cooling curve at the time of constituting the upper layer of a gate electrode from a material with comparatively low thermal conductivity according to this invention. This cooling curve (2) is approaching the cooling curve (3) so that clearly from a graph. That is, according to this invention, time difference after the silicon on glass and the silicon on a gate electrode carry out melting until it solidifies can be made small. It is easy to be able to obtain the silicon of a crystallized state almost uniform irrespective of a difference of a substratum by this, and to optimize the conditions of laser annealing.

[0020] Drawing 4 is process drawing showing other examples of the formation technique of the gate electrode 5. As shown in (A), sputtering of the metal membrane used as lower layer 5b is carried out on the insulating substrate 1 which consists of glass etc. For example, Ti is formed by the thickness of 200nm as a metal membrane. Next, as shown in (B), patterning of the lower layer 5b is carried out to the configuration of a gate electrode. Furthermore, as shown in (C), the front face of lower layer 5b is reformed, and upper 5a is prepared. That is, upper 5a which consists of TiN is formed by heat-treating lower layer 5b in the nitrogen ambient atmosphere. Thus, the gate electrode 5 which has the multilayer structure which piled up upper 5a and lower layer 5b is obtained. The following processes are the same as that of drawing 2 .

[0021] Drawing 5 is a typical fragmentary sectional view showing the 2nd operation gestalt of the thin-film-semiconductor equipment concerning this invention. A corresponding reference number is given to the fraction which corresponds with the 1st operation gestalt shown in drawing 1 , and understanding is made easy. Also with this operation gestalt, accumulation formation of TFT 3 of the bottom gate structure which carried out the laminating of the gate electrode 5, the insulator layer 4, and the semiconductor thin film 2 to order from the bottom is carried out on the insulating substrate 1. As a characteristic feature matter, the thermally conductive substratum layer 20 is formed in the front face of an insulating substrate 1 which consists of glass etc. so that it may see superficially and the gate electrode 5 may be adjoined, and the heat-conduction status of insulating-substrate 1 front face is made uniform. By this relation, the gate electrode 5 serves as single-level-metal layers, such as Cr, Mo, and Ta. On the other hand, the substratum layer 20 consists of transparent electric conduction layers, such as ITO. The semiconductor thin film 2 is in the status which extended on the gate electrode 5 and the substratum layer 20 through the insulator layer 4, and has the polycrystal structure in which the recrystallization was carried out by energy irradiation of a laser beam etc. As mentioned above, with this operation gestalt, in bottom gate type TFT, when carrying out recrystallization processing of the semiconductor thin film 2 by laser annealing, in order to make a heat distribution uniform, the substratum layer 20 which has thermal conductivity bigger than glass is formed in the surroundings of the gate electrode 5. Thereby, good polycrystal structure can be acquired.

[0022] Drawing 6 is a typical perspective diagram showing an example of the active matrix liquid crystal display assembled

considering the thin-film-semiconductor equipment concerning this invention as a drive substrate. This display has the structure holding the electrooptic material 50 which consists of liquid crystal etc. between the drive substrate 1 and the opposite substrate 60. Accumulation formation of the pixel array section and the circumference circuit section is carried out at the drive substrate 1. The circumference circuit section is divided into the vertical-scanning circuit 41 and the horizontal scanning circuit 42. Moreover, the terminal electrode 47 for external connection is also formed in the upper-limit side of the drive substrate 1. Each terminal electrode 47 is connected to the vertical-scanning circuit 41 and the horizontal scanning circuit 42 through wiring 48. The gate wiring 43 and the signal wiring 10 which cross mutually are formed in the pixel array section. The gate wiring 43 is connected to the vertical-scanning circuit 41, and the signal wiring 10 is connected to the horizontal scanning circuit 42. TFT 3 which drives the pixel electrode 14 and this is formed in the intersection of both wirings 43 and 10. On the other hand, the counterelectrode is formed although not illustrated to the internal surface of the opposite substrate 60.

[0023]

[Effect of the Invention] As explained above, according to the 1st side face of this invention, the gate electrode has the multilayer structure which piled up the upper layer equipped with conductivity required in order that thermal conductivity may take a low contact comparatively, and the lower layer which thermal conductivity equipped with high and conductivity required as a wiring comparatively. It is enabled to present the polycrystal structure in which receives energy irradiation and the recrystallization was carried out uniformly and the optimum by the starting configuration after the semiconductor thin film had extended on the gate electrode and the insulating substrate through the insulator layer. Moreover, according to the 2nd side face of this invention, the thermally conductive substratum layer is formed so that it may see superficially on the surface of an insulating substrate and a gate electrode may be adjoined, and the heat-conduction status on the front face of an insulating substrate is made uniform. A semiconductor thin film receives energy irradiation in the status that it extended on the gate electrode and the substratum layer through the insulator layer, and the polycrystal structure by which the recrystallization was carried out uniformly and the optimum is acquired.

[Translation done.]

L Number	Hits	Search Text	DB	Time stamp
1	65	thin adj film adj transistor and bottom adj gate same thickness	USPAT	2002/04/26 14:20
4	11	thin adj film adj transistor and gate same "90 nm"	USPAT	2002/04/26 15:11
5	36	thin adj film adj transistor and (gate adj electrode near3 nm) and (gate adj insulating adj film near3 nm)	USPAT	2002/04/26 14:57
6	62	thin adj film adj transistor and (gate adj electrode near4 nm) and (gate adj insulating near4 nm)	USPAT	2002/04/26 14:58
7	62	thin adj film adj transistor and bottom adj gate same polycrystalline adj silicon	USPAT	2002/04/26 15:35
8	22	thin adj film adj transistor and gate adj electrode same Al near3 Mo near3 ta near3 w	USPAT	2002/04/26 15:43
9	37	thin adj film adj transistor and gate adj electrode near3 multi$1layer	USPAT	2002/04/26 16:17
23	2	jp-10209467-$.did.	JPO; DERWENT	2002/04/26 16:31
-	2144	(257/59,64-66,70,72,75,347).CCLS.	USPAT	2002/04/26 10:08